



Forum on specification & Design Languages

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• Location

FDL 2026 is hosted by Guglielmo Marconi University, Via Plinio 44, 00193 Rome, Italy.
<https://www.fdl-conference.com/venue.html>

• Welcome Reception

Wednesday, September 9, from 7:00 pm at Baja Roma (Lungotevere Arnaldo da Brescia). Transfer from the university at 6:30 pm.

• Social Event

Thursday, September 10, from 5:30 pm: visit to the Capitoline Museums, followed by the conference dinner.

• Summer School

September 8, 2026: invited talks and hands-on tutorials, the day before the conference.

	09.09	10.09	11.09
	WEDNESDAY	THURSDAY	FRIDAY
8:30	Registration		
9:00		Keynote 2	Keynote 3
9:30	Opening Remarks		
10:00	Keynote 1	Panel	Tutorial 2
10:30			
11:00	Coffee Break	Coffee Break	Coffee Break
11:30			
12:00	Session 1	Session 3	Session 5
12:30			
13:00	Lunch *	Lunch	Lunch
13:30			
14:00			Session 6
14:30	Special Session 1	Session 4	
15:00			Closing Remarks / Best Paper
15:30	Coffee Break	Coffee Break	
16:00	Session 2	Tutorial 1	
16:30			
17:00		Transfer	
17:30	Special Session 2		
18:00			
18:30	Transfer		
19:00		Social Event	
19:30	Welcome Reception		
20:00			

SS1: Architectures and Methods for Trustworthy On-Device Computation

SS2: Hardware Construction Languages - RTL on Steroids

* PhD / WiP / Poster Forum: posters on display at the conference venue

Full program and updates: www.fdl-conference.com

September 9-11, 2026
Rome, Italy



KEYNOTE SPEAKERS

Peter Lieber

Sparx Systems Ecosystem

June Andronick

Proofcraft / seL4 Foundation

Gianvito Lorusso

Synopsys

CONFERENCE
PROGRAM





Forum on specification & Design Languages

September 9-11, 2026 Rome, Italy

Wednesday 9

- 08:30-09:30 **Registration**
- 09:30-10:00 **Opening remarks**
- 10:00-11:00 **Keynote 1**
 - *From Models to Decisions - Why Modeling Must Become an Execution Engine in the Age of AI*
(Speaker: Peter Lieber, Sparx Systems Ecosystem, Austria)
- 11:00-11:30 **Coffee break**
- 11:30-13:00 **Session 1**
 - *Hardware Design*
 - 1.1 SAMpLE: A SystemC-AMS Machine LEarning-based Framework for Virtual Prototyping
Andrei Mihai Albu and Sara Vinco
 - 1.2 Hardware synthesis of functional programs with Esterel constructs
Loïc Sylvestre
 - 1.3 Enabling Cross-Language and Cross-Level Verification Reuse Using SCVPI
Bhavay Arora, Rainer Dorsch and Christian Haubelt
 - 1.4 A Breath of Fresh AIR: Programmatic Construction for SystemC
Rainer Doerner
- 13:00-14:00 **Lunch + Poster Forum**
- 14:00-15:30 **Special Session 1**
 - *Architectures and Methods for Trustworthy On-Device Computation*
(Organizers: Salvatore Bramante, IMT School for Advanced Studies Lucca; Francesco Vitale, University of Naples Federico II; Matteo Busi, Ca' Foscari University of Venice, Italy)
- 15:30-16:00 **Coffee break**
- 16:00-17:00 **Session 2**
 - *Design Verification and RISC-V*
 - 2.1 Exploring the Parameter Space for Constrained Random Verification of RISC-V CPUs
Sallar Ahmadi-Pour, Luca Müller and Rolf Drechsler
 - 2.2 FP-RVVTs: Sail-guided Verification of RISC-V Floating-Point Implementations
Katharina Ruep, Manfred Schlögl and Daniel Grosse
 - 2.3 FITS: Towards Automatic Open-Source IP Integration
Anton Paule, Robert Kunzelmann, Markus Leibl, Johannes Geier, Stefan Wallentowitz, Wolfgang Ecker and Ulf Schlichtmann
- 17:00-18:30 **Special Session 2**
 - *Hardware Construction Languages: Register Transfer Level on Steroids*
(Organizer: Frédéric Pétrot, Univ. Grenoble Alpes, CNRS, Inria, Grenoble INP, TIMA, France)
- 18:30-19:00 **Transfer to Baja Roma**
- from 19:00 **Welcome reception**
 - *Baja Roma - a barge moored on the Tiber*
Lungotevere Arnaldo da Brescia, 00196 Rome - www.bajaroma.it

Thursday 10

- 09:00-10:00 **Keynote 2**
 - *seL4: the journey of a verified kernel deployed in real systems*
(Speaker: June Andronick, Proofcraft / seL4 Foundation)
- 10:00-11:00 **Panel**
 - *The Virtual Prototype (VP) is Dead - Why do we invest so much effort in something that is rarely used?*
(Organizer: Wolfgang Ecker, Infineon Technologies, Germany)
Panelists: Rainer Doerner, Franco Fummi, Daniel Große, Wolfgang Müller, Jan-Hendrik Oetjens
- 11:00-11:30 **Coffee break**
- 11:30-13:00 **Session 3**
 - *Circuit and Neural Network Verification*
 - 3.1 Scalable Verification for Dot-Product Architectures using Symbolic Computer Algebra
Lennart Weingarten, Kamalika Datta and Rolf Drechsler
 - 3.2 Formally Verifying Analog Neural Networks Under Process Variations Using Polynomial Zonotopes
Yasmine Abu-Haeyeh, Tobias Ladner, Matthias Althoff and Lars Hedrich
 - 3.3 Polynomial Formal Verification of Structurally Simple Multipliers
Jan Kleinekathöfer, Lennart Weingarten, Kamalika Datta and Rolf Drechsler
 - 3.4 FormalHandshake - Open Source Design and Verification Flow for complex Hardware Circuits
Milan Funck, Christoph Lüth and Rolf Drechsler
- 13:00-14:00 **Lunch**
- 14:00-15:30 **Session 4**
 - *Machine Learning: Specification and Applications*
 - 4.1 Modeling Neural Networks in SysML v2: Introducing Performance Constraints in OpenBoardnet
Sebastian Post, Hagen Heermann and Christoph Grimm
 - 4.2 Relaxed activation analysis of dataflow networks: A clock calculus for machine learning
William Gaudelieu, Dumitru Potop Butucaru and Albert Cohen
 - 4.3 TIPster: Zero-Shot Anomaly Detection via Language-Steered Anomaly Informed Patches
Uzair Khan, Luigi Capogrosso, Michele Magno, Franco Fummi and Marco Cristani
 - 4.4 Embodied AI Launcher: A Tool for Modeling, Simulation, and Deployment Evaluation of Transformer-Based Embodied AI Tasks at the Edge
Byeonggil Jun, Deeksha Prahlad, Mehdi Ghasemi and Hokeun Kim
- 15:30-16:00 **Coffee break**
- 16:00-17:00 **Tutorial 1**
 - *On Languages, Models, and Modelled Items*
(Wolfgang Ecker, Infineon Technologies / TU Munich, Germany)
- 17:00-17:30 **Transfer to the social event**
- 17:30-23:00 **Social event**
 - *Rome by night: visit to the Capitoline Museums, followed by the conference dinner*

Friday 11

- 09:00-10:00 **Keynote 3**
 - *Re-engineering EDA in the Era of Pervasive Intelligence*
(Speaker: Gianvito Lorusso, Synopsys, Italy)
- 10:00-11:00 **Tutorial 2**
 - *Let's Scratch the Surface of the SysML v2 Meta Model*
(Sebastian Reiter, FZI Research Center for Information Technology, Germany)
- 11:00-11:30 **Coffee break**
- 11:30-13:00 **Session 5**
 - *Cyber Physical Systems*
 - 5.1 NAS-in-the-Loop: Trajectory-driven Neural Architecture Search for Safe Autonomous CPS
Zayah Cortright, Prateek Ganguli, Tingan Zhu and Samarjit Chakraborty
 - 5.2 Refining Timing Uncertainty from Logical Time Specification to Operation
Pavlo Tokariev and Julien Deantoni
 - 5.3 MakSafe: A Spatiotemporal Semantic Framework for Formal Specification and Compliance Checking of Road Vehicle Safety Rules
Maksym Labzhaniia, Julien Deantoni, Marie-Agnès Peraldi-Frati and Frédéric Mallet
 - 5.4 From DNN Perception Accuracy to Physical Safety: ML/Architecture Co-Design for Autonomous CPS
Oliver Bringmann and Samarjit Chakraborty
- 13:00-14:00 **Lunch**
- 14:00-15:00 **Session 6**
 - *Design Space Optimization*
 - 6.1 Simultaneous Topology and Control Exploration for Manufacturing Systems
Daniel Sarsur, Patricia Nascimento Pena, Lucas Alves, Martijn Goorden and Michel Reniers
 - 6.2 LLM-Guided Design Space Exploration for Neural Network Accelerators on FPGA
Edoardo Trombotto, Valentino Peluso, Andrea Calimera and Enrico Macii
- 15:00-15:30 **Closing remarks / Best Paper Award**

Summer School, September 8

Talks: Daniele Passaretti (OvGU Magdeburg); Wolfgang Ecker (Infineon / TU Munich); Sebastian Reiter (FZI Karlsruhe).
Hands-on: Hokeun Kim (Lingua Franca); Enrico Fraccaroli (GLACIER); Frédéric Pétrot (Chisel).

**Most up-to-date
information**

www.fdl-conference.com



Program updates: fdl-conference.com